(19) World Intellectual Property Organization International Bureau



(43) International Publication Date 17 February 2005 (17.02.2005)

PCT

(10) International Publication Number WO 2005/015532 A1

(51) International Patent Classification7:

G09G 3/36

(21) International Application Number:

PCT/IB2004/002586

(22) International Filing Date:

30 July 2004 (30.07.2004)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

0318611.1

8 August 2003 (08.08.2003) GB

(71) Applicant (for all designated States except US): KONIN-KLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

- (75) Inventors/Applicants (for US only): EDWARDS, Martin, J. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).
 AYRES, John, R., A. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).
- (74) Agent: WILLIAMSON, Paul, L.; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,

PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

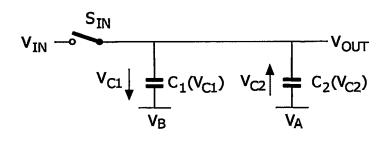
as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CIRCUIT FOR SIGNAL AMPLIFICATION AND USE OF THE SAME IN ACTIVE MATRIX DEVICES



(57) Abstract: An amplification circuit comprises a capacitor arrangement (42) and a switching arrangement. The capacitor arrangement has a first capacitor (C2) which has a voltage-dependent capacitance and a second capacitor (C1) (which may also be voltage-dependent). The circuit is operable in two modes, a first mode in which the input voltage is provided to one terminal of at least the first capacitor, and a second mode in which the switching arrangement causes charge to be redistributed between the first and second

capacitors such that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor, the output voltage being dependent on the resulting voltage across the first capacitor. The invention uses a voltage controlled capacitance in combination with charge sharing between capacitors, which has the result of providing a voltage amplification characteristic. This arrangement can thus be used for the amplification of an analogue voltage, or the boosting of a fixed level (i.e. digital voltage). Thus, the circuit of the invention can be used for level shifting or amplification, for example for use in the pixels of an active matrix array device.

7 2005/015532 A1